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A novel high-performance complete fully differential two-stage cascade amplifier in bipolar transistor implementation

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Abstract: We present a novel, universal architecture for a cascade linear symmetric fully differential amplifier. It is applicable to all implementation sets of complementary pair devices such as BJT, JFET, MOSFET. The presented examples demonstrate the superiority of the proposed circuit over the existing solutions. Comparison of the proposed and the traditional differential amplifier is done under the same quiescent conditions and with the same set of complementary npn-pnp devices. Characteristics are illustrated in frequency and time domain, and it is also given linearity error of voltage transfer characteristic amplifier. A common mode gain of the proposed amplifier with a double-ended output is negligible because the new structure is inherently fully symmetric. Prospective applications of the proposed amplifier include permanent monitoring of the natural phenomena, audio signals of speech and music, and also various signals in medicine, pharmacy, science, technique and other areas.

Linearity error of the static voltage transfer characteristic of the novel amplifier is 0.0072 mV for 1 Vpp of the output signal. Classical amplifier produces significantly higher linearity error of 19.24 mV for output voltage swing of 0.86 Vpp.

Proposed design strategy of operational amplifiers employing new complete fully differential amplifier will have application in processing of differential real signal in s domain and also real and complex sequences in z domain, special audio and RF signal.

Keywords: Complete fully differential amplifier, Analogy electronic, Clear factor distortion, Linearity error, Audio processing, Audio frequency amplifiers

1 Introduction

Sixty years since bipolar transistor invention we have proposed a new universally structure for fully linear cascade differential amplifier which is applicable for any set of complementary pair devices BJT, JFET, MOSFET respectively implemented in any technology.

In the work [1] is described complete methodology and systematic approach for detailed analysis, classification and design of the classical differential amplifier with current mirror

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load (the most important amplifier generally). This amplifier is distinguished by nonsymmetrical characteristics for an obvious reason that it has short-circuited base and collector on only one transistor in active load of the basic differential pair.

Multistage and one-stage diferential amplifier topologies are an actual research subject [2 - 3] because of their extremely wide application in integrated circuits. Differential amplifier is compatible with integrated circuit technology and is very versatile circuit in analog circuit design [4 - 6]. Some of the broad successful applications of the important classical differential amplifier employed in the scope of system for analog and digital signal processing can be found in [7 - 12]. Some of applications are also described in literature [13 - 20].

In paper [21] low frequency $1/f$ noise in MOS and bipolar transistors is described as an important figure-of-merit in design analog RF and microwave circuits, because it places a fundamental limit on the achievable spectral purity of a system. Not only is $1/f$ noise important for low frequencies, but it can also impact high frequency applications. For example, intrinsic low-frequency noise can be up-converted in RF mixers, oscillators, and power amplifiers due to non-linearity in the devices.

The $1/f$ noise in MOS transistors is the result of Si/SiO2 interface states resides within the gate oxide regions of the MOSFETs. These near channel electronic states are capable of modulating the channel charge and hence the channel conductance. In contrast, the bipolar transistors have lower $1/f$ noise than their counterpart MOS transistors. This occurs due to the bulk conduction nature of bipolar devices in comparison to surface channel conduction for MOSFET devices.

In literature [21] that advantage is illustrated in Fig. 1, which shows a normalized collector current and drain current spectral noise density denoted as S_{IC} and S_{ID} , respectively, versus drawn emitter and gate areas. It indicates that for a given active MOSFET gate area and identical active emitter bipolar area, the bipolar transistors will have lower $1/f$ noise for a given drive current.

In the Figs. 1 and 2 are given first and second stage of the classical two-stage differential amplifier.

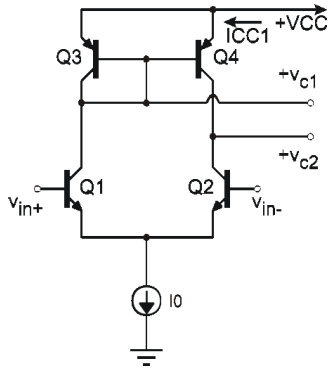

Fig. 1. Schematic of the first stage cascade of the classical differential amplifier

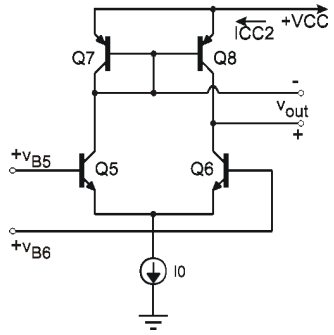

Fig. 2. Schematic of the second stage cascade of the classical differential amplifier

This paper presents novel, original scheme for a symmetric fully two-stage cascade differential amplifier. Analysis and comparison of the classical and proposed amplifier are given by using simulation technique in time and frequency domain and also voltage transfer characteristic linearity analysis.

The superiority and perspective of the proposed differential amplifier structure will be emphasized by using negative feedback. The authors expect superiority and perspective of the properly combined system by using negative feedback and fully differential symmetric amplifier structure with active load configuration, , because of a high gain-bandwidth product. The authors also expect that dominant influence of negative feedback in new operation amplifiers will be exploited in a wide variety of applications with very high requirements and very low distortions.

2 Total two-stage cascade balanced symmetric fully differential bipolar amplifier

A new original topology of fully cascade differential amplifier using common mode emitter proposed in this work is illustrated in Fig. 4 and Fig. 5. Given identical transistors are NPN 2N3904 and PNP 2N3906 respectively.

For the analysis of the topology, it is considered the input signal to be composed by differential and common-mode signal components, which are applied at the inputsv_{in+}, v_{in-}.

The symmetrical output voltage, $v_{out}(s)$, of the fully differential amplifier shown in Fig. 4 and Fig. 5 has a representative expression form in Laplace, s, domain [22]

$$v_{out}(s) = v_{C8}(s) - v_{C7}(s) = A_d(s) \cdot (v_{in+} - v_{in-}) + A_c(s) \cdot (v_{in+} + v_{in-}) \tag{1}$$

where particular gains are: double-ended differential gain, $A_d(s)$, and double-ended common-mode gain, $A_c(s)$, given by definition expression. The idealized differential amplifier should have $A_d(s) >> 1$, and $A_c(s) \to 0$.

The desired differential, $A_d(s)$ and undesired, parasitic common-mode, $A_c(s)$ gain for fully symmetric balanced two-stage differential amplifier can be analyzed using small-signal models and are given by:

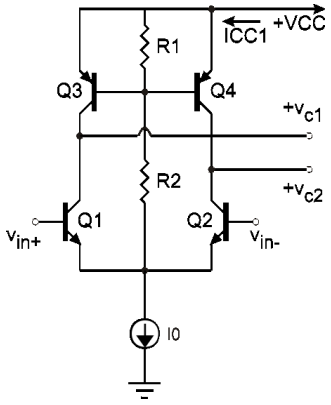

Fig. 3. Schematic of the first stage of the new symmetrical fully two-stage differential bipolar amplifier

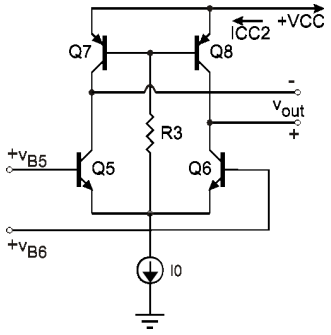

Fig. 4. Schematic of the second stage of the new symmetrical fully two-stage differential bipolar amplifier

$$A_d(s) = \frac{v_{out}(s)}{v_{C2}(s) - v_{C1}(s)} \cdot \frac{v_{C2}(s) - v_{C1}(s)}{v_{in+}(s) - v_{in-}(s)} = A_{d2}(s) \cdot A_{d1}(s) \tag{2}$$

$$A_c(s) = \frac{v_{out}(s)}{v_{C2}(s) + v_{C1}(s)} \cdot \frac{v_{C2}(s) + v_{C1}(s)}{v_{in+}(s) + v_{in-}(s)} = A_{c2}(s) \cdot A_{c1}(s) \tag{3}$$

Parasitic, undesired common-mode gain$A_c(s)$, should have as smaller value as possible $Re\{A_c(j\omega)\} \to 0 \quad Im\{A_c(j\omega)\} \to 0$**.**

The main intention of the novel, fully two-stage differential amplifier is to accomplish as higher $A_d(s) = A_{d2}(s) \cdot A_{d1}(s)$, for any components type and any technology, in the contest of absolutely constant expanding into a series [23], while that value should be constant in the pass-band.

The main idea in this work is minimization of the numerical value$A_c(s)$, namely minimization of both factors,$A_{c2}(s)$, $A_{c1}(s)$ practically as much as possible, so that corresponding component of the output voltage numerical value is negligible. The classical differential amplifier with active current mirror load has unavoidable nonzero $A_c(s)$.

The initial idea for the proposed original symmetric structure of the fully differential amplifier is generated by detailed analysis of works [23, 24, 25].

We studied the influence of the expanding the constant into a series and the influence of the numerical accuracy function in interval infinity. These two influences we have incorporated in the novel structure of Figs. 4 and 5 and obtain expected improvements of all circuit characteristics. The dominant node of the differential amplifier is the node of shortcut basic differential pair (NPN type 2N3904), Q1 and Q2 (Q7 and Q8) of two sources, which generated the main effects and characters of the circuit. That part of the circuit makes a great difference for common-mode and differential-mode signals and this work emphasizes that property.

In the paper [23] a new technique has been demonstrated that includes direct application of set of non-periodic classical orthogonal polynomials generating function for determining prototype non-monotonic filter functions. Starting from absolute expansion of the constant into a series, filter function is obtained directly in a compact form, by simply breaking-off absolute development while that function always has N flatness conditions for the amplitude characteristics at the coordinate origin, independent on the type of classical orthogonal polynomial and independent on the free parameter value. [23 - 25]

3 Analysis and performance of balanced symmetric fully cascade differential amplifier

Validity of the results is usually performed by the simulation. Electronic circuit simulation provides insight into behavior of electronic circuit design and greatly improves fabrication efficiency. The intention of the work is validation of the proposed circuit configuration. Therefore the proposed circuit configuration is analyzed using discrete bipolar components in order to reduce parasitic effects and decrease circuit complexity as much as possible.

Negative feedback improves circuit performance and reduces influence of manufacturing or environmental process variations on circuit performance, which allows chip manufacturers to increase production [26 - 29].

Some parameters of the first stage of the classical and novel differential amplifiers are given in Table I.

Table 1. Parameters of the first stage of the cascade differential amplifiers

Some Parameters first stage differential amplifier	Novel	Classic
Collector current, Ic2 (T1=25^0C) (mA)	0.1269	0. 1275
Collector current, Ic2 (T2=$55\ ^0$ C) (mA)	0.128	0.1287
Double-ended input, double ended output common mode gain, Ac	$0.00\ 10^{-9}$	$7.83\ 10^{-6}$
Double-ended input, double ended output differential gain, Ad (dB)	9.0251	7.71
Phase margin, PM (deg)	118.26	129.48
Gain margin, GM (dB)	-17.3	-26
3dB frequency, $f_{3dB,}$(kHz)	202.1	161.92

Figures 6 and 7 show comparison of characteristics of the classical and proposed two-stage amplifier in time and frequency domain under the same direct current (DC) regime.

Improvements of characteristics of the proposed cascade amplifier are obvious from

Figs. 6 and 7 and also from some of simulation results numerically expressed in the Table II. It is worth noting that common mode gain of the proposed fully differential symmetric voltage amplifier is theoretically equal to zero, because both collectors of the basic differential pairs (Q1, Q2 and Q7, Q8) have identical loads.

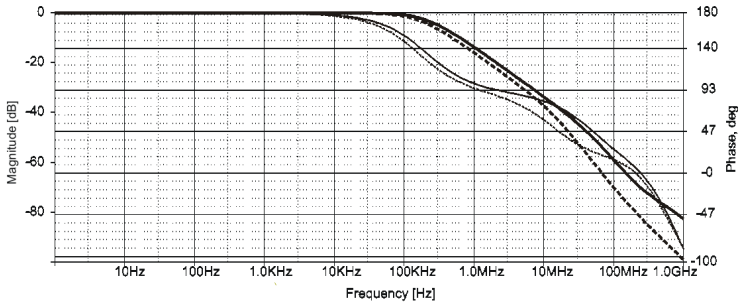

Fig. 5. Normalized magnitude and phase responses

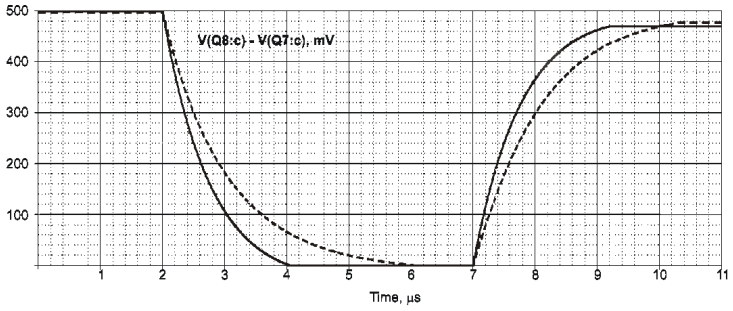

Fig. 6. Step responses

Table II summarizes simulation results and compare the performance of the two-stage cascade differential amplifiers respectively.

Fig. 8 shows the pulse response to step input signal and 1 Vpp output signal. From this diagram we estimate positive and negative slew rate equal to 0.290 V/μS and 0.292 V/μS respectively, which is more than 40 % higher value than the result of the classical amplifier.

Table II presents comparison between the classical and proposed amplifier including positive and negative slewrate. The improvement realised by the proposed amplifier is obvious.

Table 2. Summated parameters of the two-stage cascade differential amplifiers

Some total parameters two-stage cascade differential amplifier	Novel	Classic
Collector current, Ic8 (T1=25^0 C) (mA)	8.68	9.488
Collector current Ic8 (T2=55^0 C) (mA)	8.925	9.558
Double-ended input, double ended output common-mode gain, Ac	0.00 10^{-6}	3.877 10^{-3}
Double-ended input, double ended output differential gain, Ad (dB)	64.96	61.66
Phase margin, PM (deg)	6.41	
Gain margin, GM (dB)	-2.79	
3dB frequency, f_{3dB} (kHz)	199.01	159.056
Gain-bandwith product, GBW (MHz)	742.61	472.66
Positive (Negative) Slew Rate, SR (V/μS)	0.290 / 0.292	0.219 / 0.212
Harmonic distortion coefficient, K2@Vopp		7.04 10^{-3} / 0.5 V
Harmonic distortion coefficient, K3@Vopp		4.51 10^{-3} / 0.5 V
Harmonic distortion coefficient, K4@Vopp		2.54 10^{-3} / 0.5 V
Harmonic distortion coefficient, K5@Vopp		1.11 10^{-3} / 0.5 V
Harmonic distortion coefficient, K3@Vopp	0.171 10^{-3} / 5 V	
Harmonic distortion coefficient, K3@Vopp	0.437 10^{-3} / 8 V	
Harmonic distortion coefficient, K3@Vopp	0.65710^{-3} / 10 V	

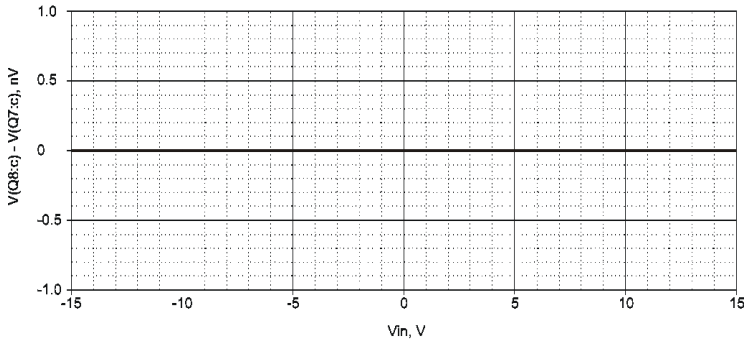

Fig. 7. AC common-mode double ended static voltage transfer characteristic of the proposed amplifier

4 Analysis of the active range and linearity voltage transfer characteristic differential cascade amplifier

It is worth noting that the common mode gain of the proposed amplifier is zero because both collectors of the differential pair (Q1, Q2 and Q7, Q8) have identical load.

A new original differential amplifier naturally produces extremely small common-mode gain, as a result of completely symmetrical differential pair active load. Fig. 8 shows output voltage in function of common-mode input voltage in the range of -15 V to 15 V. The output voltage has extremely small value of 0.0 nV. It is worth noting the important realized new surpassed result that common-mode gain of the proposed fully differential symmetric

voltage amplifier with accurately balanced outputs is equal to zero, because both collectors differential pair (Q1, Q2 and Q7, Q8) have identical load.

Fig. 9 shows comparison between differential-mode static voltage transfer characteristics of the proposed and the classical differential amplifier. Advantages and quality of the proposed structure are obvious. The classical amplifier has dynamic range of output voltage always small and independent than the numerical value of the voltage source V_{CC}. The proposed amplifier has output swing much higher than the classical one and it is only limited by the numerical value of voltage supply.

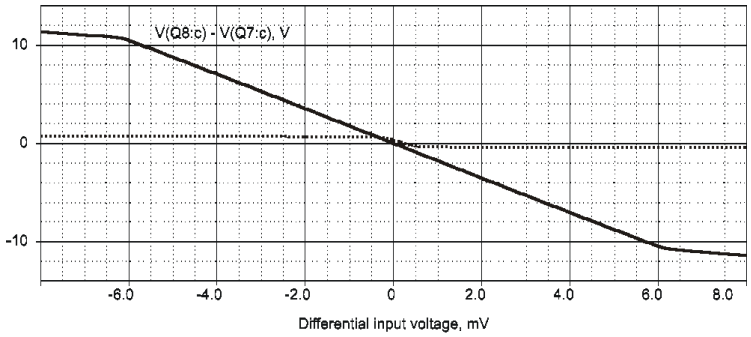

Fig. 8. AD differential mode double ended static voltage transfer characteristics

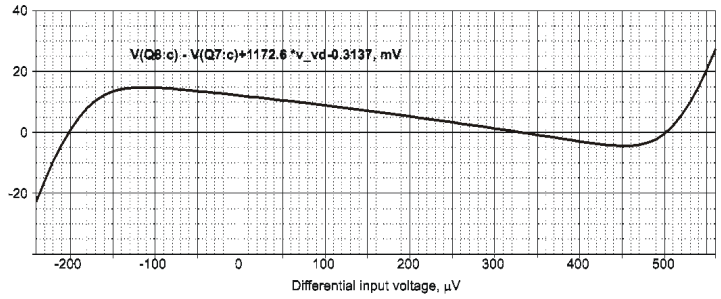

Fig. 9. Linearity error of the static differential-mode double-ended voltage transfer characteristic of the classical solution $\max V_{in\ peaktopeak} = 0.88\ V_{pp}$

Figs. 10 and 11 show linearity error of the differential-mode static voltage transfer characteristic for the classical and proposed differential amplifier respectively.

Fig. 11 shows linearity error of the proposed amplifier static voltage transfer characteristic for the output voltage swing of 1 V peak-to-peak. We emphasize that classical differential amplifier has linearity error in active region of about 19.24 mV, and the novel proposed solution of the amplifier only 0.0072 mV for the approximately same output signal level.

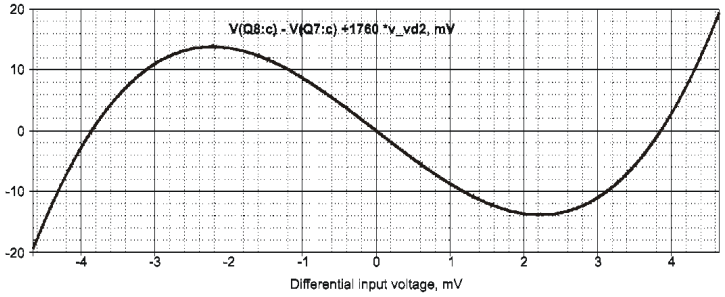

Fig. 10. Linearity error of the static differential-mode double-ended voltage transfer characteristic of the proposed solution $V_{in} = 17.6\,V_{pp}$

In the Fig. 12 it is shown zoomed linearity error of the voltage transfer characteristic of the proposed solution $V_{in} = 1\,V_{pp}$

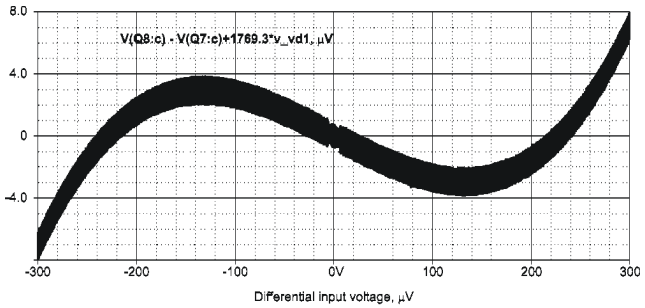

Fig. 11. Zoomed linearity error of the voltage transfer characteristic of the proposed solution $V_{in} = 1\,V_{pp}$

The analysis of linearity of the proposed amplifer has also been done for the reduced output voltage swing. The slope of the the approximate straight line of the voltage-voltage transfer characteristic around a selected *DC* operating point is graphically designated for each input voltage range. Obtained quantized set of numerical linearity errors for assigned output voltage swings are given in the Table II, using the numerical value of graphically determined limiting input voltage range as the starting point.

General analytic expression of the nonlinear amplifier output voltage [30] can be expressed for the prescribed set operating points of the transistors in differential pairs of the first and the second stage as:

$$\begin{aligned} v_{out}(t)\,|_{V_{CE1},V_{CE2},V_{CE7},V_{CE8}} \quad = \quad & a_1(j\omega)v_{in}(t) + a_2(j\omega)v_{in}(t)^2 + \\ & a_3(j\omega)v_{in}(t)^3 + \ldots + a_r(j\omega)v_{in}(t)^r + \ldots \end{aligned} \tag{4}$$

Where $a_1(\,j\omega\,),\ a_2(\,j\omega\,),\ a_3(\,j\omega\,),\ldots,a_r(\,j\omega\,)$ are the first-, second-, third-,..., r-th order nonlinearity transfer function,

$$
\begin{aligned}
v_{out}(t)\,|_{V_{CE1},V_{CE2},V_{CE7},V_{CE8}} &= |a_1(j\omega)|\,V_{in}(j\omega)\,\cos\,[\omega t+\arg(a_1(j\omega)\,]+ \\
&+ \frac{1}{2}|\,a_2(j\omega)|\;\;V_{in}^2(j\omega)\,\cos\,[\,2\,\omega\,t+\arg(a_2(j\omega)\,]+ \\
&+ \left|\,a_3(j\omega)\,\frac{1}{4}\,\right|\,V_{in}^3(j\omega)\,\cos\,[\,3\omega\,t+\arg(a_3(j\omega)\,]+\ldots
\end{aligned}
\tag{5}
$$

Harmonic distortion factors can be expressed as:

$$
HD_2(j\omega_1)\,|_{V_{CE1},\,V_{CE2}\,,\,V_{CE7}\,,\,V_{CE8}} \approx \frac{1}{2}\,u_{in}(j\omega_1)\,\left|\,\frac{a_2(j\omega_1)}{a_1(j\omega_1)}\,\right| = \frac{v_{out}(2\,\omega_1)}{v_{out}(1\,\omega_1)} \tag{6}
$$

$$
HD_3(j\omega_1)\,|_{V_{CE1},\;V_{CE2},V_{CE7},V_{CE8}} \approx \frac{1}{4}\,u_{in}^2(j\omega_1)\,\left|\,\frac{a_3(j\omega_1)}{a_1(j\omega_1)}\,\right| = \frac{v_{out}(3\,\omega_1)}{v_{out}(1\,\omega_1)} \tag{7}
$$

A new symmetrical proposed amplifier has only odd harmonic components, practically the total harmonic distortion is mainly determined by the numerical value of the third harmonic distortion coefficient.

Linear distortion are actual research subject [31 -35]. Analysis of the harmonic distortion of the optimal differential amplifier is performed under the input sinwave signal of frequency *1KHz* and for a set of output voltage amplitude. Figs. 13, 15 and results given in the Table II illustrate improvement in harmonic distortion reduction, achieved by the novel amplifier structure.

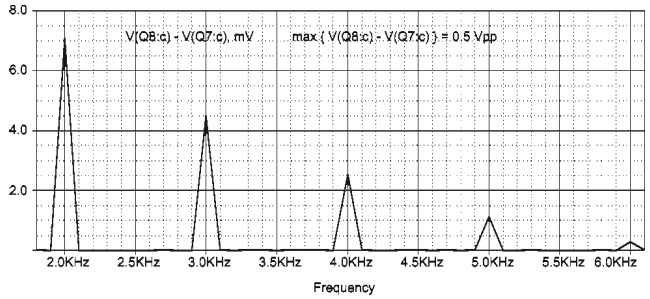

Fig. 12. Differential output clear factors spectra response for $V_o = 0.5\ V_{pp}$ differential output voltage of the classical differential amplifier

The output signal of the classical amplifier contains even and odd harmonics with amplitudes much higher than corresponding amplitudes of the proposed amplifier. Harmonic distortion of the proposed amplifier makes only odd harmonics, which small amplitudes are the consequences of the high linearity proposed amplifier for the wide range numerical value of amplitude output voltage.

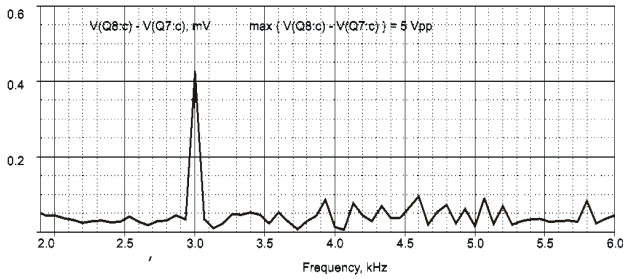

Fig. 13. Differential output clear factors spectra response for $V_o = 5.0\,V_{pp}$ differential output voltage of the proposed differential amplifier

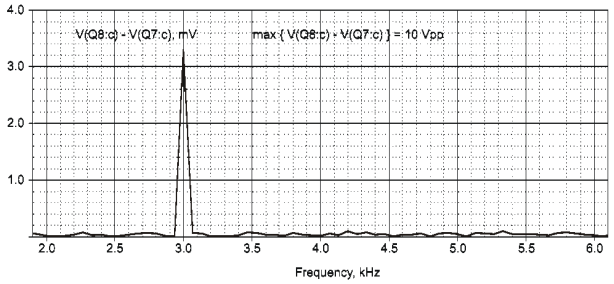

Fig. 14. Differential output clear factors spectra response for $V_o = 10.0\,V_{pp}$ differential output voltage of the proposed differential amplifier

5 Conclusion

The paper presents novel solution for the symmetrical two-stage cascade fully differential voltage amplifier. We have described the analysis and comparison and have illustrated them in the figures and tables, which give performance of the classical differential cascade amplifier with non-symmetric current mirror load and the proposed symmetric amplifier in BJT technology.

Unlike the already described amplifiers in literature, this one immediately and successfully designs for high performance and specially low linearity error of differential mode static voltage transfer characteristic if it is required.

Finally, it is worth noting that practical implementation of the proposed amplifier in design of a new generation of the analog integrated operational amplifiers for extremely performance enhancements gives new perspective for regular processing signals in nature, pharmacy, medicine, technique and other. Simulation results indicate the effectiveness and power of the proposed solution of the two-stage symmetric fully differential amplifier.

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